

The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board.

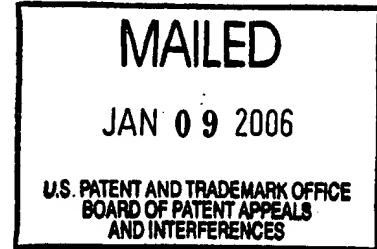
## UNITED STATES PATENT AND TRADEMARK OFFICE

### BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

*Ex parte Samson Huang*

Appeal No. 2005-1997  
Application No. 09/493,319

ON BRIEF



Before BARRY, LEVY, and MacDONALD, *Administrative Patent Judges*.

BARRY, *Administrative Patent Judge*.

A patent examiner rejected claims 45-54. The appellant appeals therefrom under 35 U.S.C. § 134(a). We affirm.

## I. BACKGROUND<sup>1</sup>

The invention at issue on appeal concerns silicon light modulators ("SLMs"). According to the appellant, many applications use SLMs. For example, a color projector may use three SLMs to modulate red, green, and blue light beams, respectively, to produce a multicolored composite image. As another example, a display for a laptop computer may include an SLM along with red, green, and blue color filters selectively mounted over the pixel cells to produce a multicolored composite image. (Spec. at 1.)

Figure 1 of the appellant's specification shows that a known SLM 1 features liquid crystal display ("LCD") pixel cells 25, which form corresponding pixels of an image. Each pixel cell 25 is part of an SLM cell 20, which also includes a capacitor 24 that stores a charge to maintain the appropriate voltage "on" the pixel cell. The SLM cells are arranged in a rectangular array 6 of rows and columns. (*Id.*) The rows are associated with row lines 14; the columns are associated with column lines 16. Each

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<sup>1</sup>An appeal "brief shall contain . . . [a] concise explanation of the invention defined in the claims involved in the appeal. . . ." 37 C.F.R. § 1.192 (c)(5)(v)(2003). Here, in the *Summary of the Invention* section of his brief, the appellant merely reproduces pages 4-7 of his specification. (Appeal Br. at 2-6.) Because such a reproduction is not a concise explanation, it fails to satisfy the aforementioned rule. We ask the examiner's help in objecting to such reproductions in the future.

pair of row lines and column lines uniquely selects an SLM cell to transfer a charge (in the form of a voltage) from a signal input line 12 to the capacitor 24 of the selected SLM cell. (*Id.* at 2.)

Because the array might be large, explains the appellant, the number of signal lines is smaller than the number of column lines. Consequently, the signal lines are used to transfer a charge to "K" SLM cells at a time (where K, the number of signal lines, is less than the M, the number of columns). Only the K column lines are driven with the new charge; the remaining column lines are held in a tri-state condition and are coupled to the unselected capacitors of the row. Unfortunately, asserts the appellant, "charge sharing typically occurs between the capacitors 24 and the tri-stated column lines 16." (*Id.* at 3.)

In contrast, Figure 2 of the specification shows the appellant's SLM cell 50. Therein, a memory 66 stores a digital indication of a pixel intensity for a pixel cell 54. A digital-to-analog converter ("DAC") 62 transforms the digital indication into an analog voltage to refresh the charge of the SLM cell's capacitor 50. As shown in Figure 3 of the specification, the SLM cell is one of several SLM cells 50 of a row. Because all the

capacitors 52 in the SLM cells of a row may be updated simultaneously, without coupling any of the capacitors to a "tri-stated" column line, asserts the appellant, charge sharing between the capacitors and the column lines does not occur. (*Id.* at 4.)

A further understanding of the invention can be achieved by reading the following claims.

45. A method comprising:

providing a light modulator comprising an array of pixel cells and memory buffers, each memory buffer being associated with a different group of two or more of the pixel cells and each memory buffer being located closer to the associated group of pixel cells than another one of the group of pixel cells; and

during a refresh operation, converting the digital indications stored in the memory buffers into analog voltages to update charge intensities on the pixel cells.

50. A light modulator comprising:

an array of pixel cells;

memory buffers being spatially distributed among the pixel cells, each memory buffer being associated with a different group of two or more of the pixel cells and storing a digital indications [sic] of associated predetermined voltages; and

digital-to-analog converters to convert the digital indications into analog voltages to update charges on the pixel cells during a refresh operation.

Claims 45-48 and 50-54 stand rejected under 35 U.S.C. § 103(a) as obvious over U.S. Patent No. 6,333,737 ("Nakajima") and U.S. Patent No. 6,297,787 ("Nishida"). (Final Rej.<sup>2</sup> at 2.) Claim 49 stands rejected under § 103(a) as obvious over Nakajima; Nishida; and U.S. Patent No. 5,771,031 ("Kinoshita"). (*Id.* at 4.)

## II. OPINION

Our opinion addresses the claims in the following order:

- claims 50-52 and 54
- claims 45-48 and 53
- claim 49.

### A. CLAIMS 50-52 AND 54

"[T]o assure separate review by the Board of individual claims within each group of claims subject to a common ground of rejection, an appellant's brief to the Board must contain a clear statement for each rejection: (a) asserting that the patentability of claims within the group of claims subject to this rejection do not stand or fall together, and (b) identifying which individual claim or claims within the group are separately

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<sup>2</sup>"We advise the examiner to copy his rejections into his examiner's answers," *Ex parte Metcalf*, 67 USPQ2d 1633, 1635 n.1 (Bd.Pat.App.& Int. 2003), rather than merely referring to a "rejection . . . set forth in a prior Office Action. . . ." (Examiner's Answer at 3.)

patentable and the reasons why the examiner's rejection should not be sustained." *In re McDaniel*, 293 F.3d 1379, 1383, 63 USPQ2d 1462, 1465 (Fed. Cir. 2002) (citing 37 C.F.R. §1.192(c)(7) (2001)). "If the brief fails to meet either requirement, the Board is free to select a single claim from each group of claims subject to a common ground of rejection as representative of all claims in that group and to decide the appeal of that rejection based solely on the selected representative claim." *Id.*, 63 USPQ2d at 1465.

Here, the appellant stipulates that "claims 50-52 and 54 can be grouped together. With this grouping, all claims of a particular group stand or fall together." (Appeal Br. at 6.) We select claim 50 from the group as representative of the claims therein.

"With this representation in mind, "[r]ather than reiterate the positions of the examiner or the appellant *in toto*, we focus on the point of contention therebetween." *Ex parte Kaysen*, No. 2003-0553, 2004 WL 1697755, at \*2 (Bd.Pat.App & Int. 2004). The examiner finds, "Nishida's teaching is that a single memory may support a groups of related pixels, such as the red, green, and blue pixels shown in Nishida, figures 8 and 10, rather than just a single pixel." (Examiner's Answer at 4.) He asserts, "This will reduce cost and complexity because, instead of one memory for only one pixel,

there would be one memory for a group of related pixels. Over a display, this would reduce the space required by the memory elements and increase the space for the light producing pixel elements." (*Id.*) The appellant makes the following arguments:

The problems and solutions that are presented in Nishida relate to reducing the possible cost associated with the mass production of individual display units do not apply to the integrated display structure that is disclosed in Nakajima. In fact, modification of Nakajima's integrated display device, as contended by the Examiner, would arguably result in more cost and complexity in Nakajima's device, as each memory 22 would serve more than one pixel. Thus, contrary to the Examiner's position, arguably cost and complexity would be added to Nakajima's display device by the proposed modification.

(Appeal Br. at 9.)

"In addressing the point of contention, the Board conducts a two-step analysis. First, we construe the representative claim at issue to determine its scope. Second, we determine whether the construed claim would have been obvious." *Ex Parte Massingill*, No. 2003-0506, 2004 WL 1646421, at \*2 (Bd.Pat.App & Int. 2004).

### *1. Claim Construction*

"Analysis begins with a key legal question — *what is the invention claimed?*" *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561, 1567, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987). In answering the question, "the Board must give claims their broadest

reasonable construction. . . ." *In re Hyatt*, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1668 (Fed. Cir. 2000). "Moreover, limitations are not to be read into the claims from the specification." *In re Van Geuns*, 988 F.2d 1181, 1184, 26 USPQ2d 1057, 1059 (Fed. Cir. 1993) (citing *In re Zletz*, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989)).

Here, claim 50 recites in pertinent part the following limitations: "each memory buffer being associated with a different group of two or more of the pixel cells" Giving the representative claim its broadest, reasonable construction, the limitations require associating a single memory with plural pixels.

## *2. Obviousness Determination*

"Having determined what subject matter is being claimed, the next inquiry is whether the subject matter would have been obvious." *Massingill*, at \*3. The question of obviousness is "based on underlying factual determinations including . . . what th[e] prior art teaches explicitly and inherently. . . ." *In re Zurko*, 258 F.3d 1379, 1383, 59 USPQ2d 1693, 1696 (Fed. Cir. 2001) (citing *Graham v. John Deere Co.*, 383 U.S. 1, 17-18, 148 USPQ 459, 467 (1966); *In re Dembicza*k, 175 F.3d 994, 998, 50 USPQ 1614, 1616 (Fed. Cir. 1999); *In re Napier*, 55 F.3d 610, 613, 34 USPQ2d 1782, 1784

(Fed. Cir. 1995)). "A *prima facie* case of obviousness is established when the teachings from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art." *In re Bell*, 991 F.2d 781, 783, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993) (quoting *In re Rinehart*, 531 F.2d 1048, 1051, 189 USPQ 143, 147 (CCPA 1976)).

Here, Nakajima "relates to a liquid crystal display device. . ." Col. 1, II. 7-8. More specifically, "[t]he liquid crystal display device 1 shown in FIG. 2 . . . comprises a display area 3 comprising a number of pixels 2. . ." Col. 2, II. 52-55. As noted by the appellant, "[t]his device includes memory and control circuitry (see Figure 1, for example) for each pixel of the device." (Appeal Br. at 7.) More specifically, the reference discloses that "not only the driving element and the storage capacitor, but also an input register circuit 21, a memory 22, an operation circuit 23, an output register circuit 24 and a digital-to-analog conversion circuit (hereinafter referred to as 'DAC circuit') 25 are integrated on the element-formed layer 8 of each pixel as shown in FIG. 1. . ." Col. 3, II. 11-17.

"The presence or absence of a motivation to combine references in an obviousness determination is a pure question of fact." *In re Gartside*, 203 F3d 1305,

1316, 53 USPQ2d 1769, 1776 (Fed. Cir. 2000) (citing *In re Dembiczak*, 175 F.3d 994, 1000, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999)). A suggestion to combine teachings from the prior art "may be found in explicit or implicit teachings within the references themselves, from the ordinary knowledge of those skilled in the art, or from the nature of the problem to be solved." *WMS Gaming Inc. v. Int'l Game Tech.*, 184 F.3d 1339, 1335, 51 USPQ2d 1385, 1397 (Fed. Cir. 1999) (citing *In re Rouffet*, 149 F.3d 1350, 1355, 47 USPQ2d 1453, 1456 (Fed. Cir. 1998)).

Here, Nishida "relates to a display device. . . ." Col. 1, l. 4. As admitted by the appellant, "[i]n lines 43-60 in column 13 of Nishida, Nishida states that a particular display unit may include several pixels that share the same . . . memory." (Appeal Br. at 8.) Furthermore, the reference recognizes that when the "structure of a display device becomes complicated," col. 1, ll. 64-65, it "need[s] much labor for its manufacture and maintenance. This results in higher manufacturing costs and maintenance costs." *Id.* at ll. 64-68.

We agree with the examiner that those skilled in the art would have known that sharing a single memory among a group of pixels, rather than dedicating a separate memory to each pixel, would have reduced the total number of memories. We also

agree that those so skilled would also have known that reducing the total number of memories, would have reduced the space required by the memories. Reducing the number of memories and the space required therefor, moreover, is consistent with Nishida's goal of reducing complexity.

"[A]rgument of counsel cannot take the place of evidence." *In re Budnick*, 537 F.2d 535, 538, 190 USPQ 422, 424 (CCPA 1976) (citing *In re Schulze*, 346 F.2d 600, 145 USPQ 716 (CCPA 1965); *In re Cole*, 326 F.2d 769, 140 USPQ 230 (CCPA 1964)). Here, the appellant offers no evidence that sharing a single memory among a group of pixels "would arguably result in more cost and complexity in Nakajima's device, as each memory 22 would serve more than one pixel." (Appeal Br. at 9.) Agreeing with the examiner's finding that a person of ordinary skill in the art would have been motivated to combine teachings of Nakajima and Nishida, we affirm the obviousness rejection of claim 50 and of claims 51, 52, and 54, which fall therewith.

#### B. CLAIMS 45-48 AND 53

The appellant stipulates that claims 45-48 and 53 "can be grouped together. With this grouping, all claims of a particular group stand or fall together." (Appeal Br. at 6.) We select claim 45 from the group as representative of the claims therein.

The examiner makes the following assertions.

[O]ne in the art combining Nakajima with Nishida would locate the memory as close to the associated pixel elements as possible to minimize any space taking lead lines with their associated resistance and capacitance. One in the art would also locate the memory generally center of the pixel elements so that all pixel elements are equal distance from the memory to reduce any variation of capacitance and resistance associated with different length lead lines.

(Examiner's Answer at 4-5.) The appellant argues that "the Examiner fails to show why locating a memory buffer closer to an associated group of pixel cells than another group of pixel cells necessarily flows from the teachings of either Nakajima or Nishida."

(Reply Br. at 3.)

#### *1. Claim Construction*

Claim 45 recites in pertinent part the following limitations: "each memory buffer being located closer to the associated group of pixel cells than another one of the group of pixel cells." Giving the representative claim its broadest, reasonable construction, the limitations require locating a memory closer to the pixels that share the memory than to the pixels that do not.

*2. Obviousness Determination*

"FIG. 10 [of Nishida] is a partial front view showing the configuration of a color display 100 of a structure in which a large number of . . . display units [80] are arranged in a matrix form." Col. 10, ll. 65-67. "[I]n the embodiment shown in FIG. 10 . . . three light emitting diodes [("LEDs")] 83R, 83G, 83B are included within a single display unit 80. . . ." Col. 13, ll. 46-48. "FIG. 9 is a circuit diagram of [the] display unit 80. . . ." Col. 10, ll. 63-64. As shown in Figure 9, the three LEDs 83R, 83G, 83B share a common memory 82. Because the memory 82 is located in the same display unit 80 as the LEDs 83R, 83G, 83B that share the memory, we find that the shared memory is closer to those LEDs than to the LEDs located in other display units. When combining teachings of Nakajima and Nishida to associate a single memory being with plural pixels, we are persuaded the latter reference would have suggested locating the single memory closer to the pixels that share the memory than to the pixels that do not. Therefore, we affirm the obviousness rejection of claim 45 and of claims 46-48 and 53, which fall therewith.

#### C. CLAIM 49

Rather than separately addressing claim 49, the appellant relies on the argument he advanced for claim 45, (Appeal Br. at 11), which we have found unpersuasive *supra*. Therefore, we also affirm the obviousness rejection of claim 49.

#### III. CONCLUSION

In summary, the rejections of claims 45-49 and 50-54 under § 103(a) are affirmed.

"Any arguments or authorities not included in the brief will be refused consideration by the Board of Patent Appeals and Interferences. . . ." 37 C.F.R. § 1.192(a). Accordingly, our affirmance is based only on the arguments made in the briefs. Any arguments or authorities omitted therefrom are neither before us nor at issue but are considered waived. *Cf. In re Watts*, 354 F.3d 1362, 1367, 69 USPQ2d 1453, 1457 (Fed. Cir. 2004) ("[I]t is important that the applicant challenging a decision not be permitted to raise arguments on appeal that were not presented to the Board.") No time for taking any action connected with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED

**LANCE LEONARD BARRY**  
**Administrative Patent Judge**

STUART S. LEVY  
Administrative Patent Judge

ALLEN R. MacDONALD  
Administrative Patent Judge

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